Attorney Docket No.: CYPR-CD00232

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Warren Snyder

Serial No.: 10/033,027 Group Art Unit:

Filed: 10/01/01 Examiner:

Title: PROGRAMMABLE SYSTEM ON A CHIP

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	6,144,327	11/07/00	Distinti et al.	341	126	08/12/97
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	C	6,166,367	12/26/00	Cho	250	208.1	03/26/99
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	K	5,426,378	06/20/95	Ong	326	39	04/20/94
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	M	5,703,871	12/30/97	Pope et al.	370	248	05/26/95
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Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	T							

12/3/06

Related Pending US Patent Applications

Examiner Initial	No.	Docket Number, Title, Filing Date, Serial Number & Inventors
	U	CYPR-CD00169; "PROGRAMMABLE MICROCONTOLLER ARCHITECTURE (MIXEDANALOG/DIGITAL)"; 08/07/01; 09/924,734; Snyder et al.
	V	CYPR-CD00170; "DIGITAL CONFIGURABLE MACRO ARCHITECTURE"; 07/18/01; 09/909,045; W. Snyder
	W	CYPR-CD00172; "CONFIGURING DIGITAL FUNCTIONS IN A DIGITAL CONFIGURABLE MACRO ARCHITECTURE"; 07/18/01; 09/909,109; Snyder
	X	CYPR-CD00173; " A PROGRAMMABLE ANALOG SYSTEM ARCHITECTURE (AS AMENDED)"; 07/18/01; 09/909,047; M. Mar
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	Z	CYPR-CD00175; "METHOD FOR SYNCHRONIZING AND RESETTING CLOCK SIGNALS SUPPLIED TO MULTIPLE PROGRAMMABLE ANALOG BLOCKS (AS AMENDED)"; 10/01/01; 09/969,311; B. Sullam
	AA	CYPR-CD00180; "METHOD AND APPARATUS FOR PROGRAMMING A FLASH MEMORY"; 06/05/01; 09/875;599; W. Snyder
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Examiner		Date Considered 12/8/06

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Attorney Docket No.: CYPR-CD00232

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Snyder

Group Art Unit: 2183

Filed: October 22, 2001

Examiner: PAN, Daniel H.

Application No.: 10/033,027

Confirmation No.: 8635

Title: PROGRAMMABLE SYSTEM ON A CHIP

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U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
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Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
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	M	0499383A2	8/19/92	EPO	H03K	19/177		
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	R	Goodenough, F. "Analog Counterparts of FPGAS Ease System Design" Electronic Design, Penton Publishing Cleveland, OH, US vol. 42, no. 21, 10/14/94, pages 63-64, 66,68,7 XP000477345 ISSN: 0013-4872 the whole document.
	S	Harbaum T. El. Al: "Design of a Flexible Coprocessor Unit" Proceedings of the Euromicro Conference, XX XX, Sept. 1999, pages 335-342, XP000879556, page 337, right-hand column, line 13-page 338, left hand column, line 4; figure 1.

Examiner	Date Considered
	4/13/05

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Title: PROGRAMMABLE MICROCONTROLLER ARCHITECTURE

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	6,460,172	10/01/02	Insenser Farre et al.	716	17	06/21/00

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	B							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C	

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.